CLAIMS

What is claimed is:

1. An electrically erasable programmable memory device, comprising:

a first semiconductor layer doped with a first dopant in a first concentration;

a second semiconductor layer, adjacent the first semiconductor layer, doped with a second dopant that has an opposite electrical characteristic than the first dopant, the second semiconductor layer having a top side;

two spaced-apart diffusion regions embedded in the top side of the second semiconductor layer, each diffusion region doped with the first dopant in a second concentration greater than the first concentration, the two diffusion regions including a first diffusion region and a second diffusion region, a first channel region defined between the first diffusion region and the second diffusion region;

a floating gate, comprising a conductive material, disposed adjacent the first diffusion region and above the first channel region and separated therefrom by a first insulator region, the floating gate capable of storing electrical charge; and

a control gate, comprising a conductive material, disposed laterally adjacent the floating gate and separated therefrom by a first vertical insulator layer, the control gate being adjacent the second diffusion region and above the first channel region and separated therefrom by a second insulator region.

2. The memory device of claim 1, wherein the first dopant having a P-type characteristic and the second dopant having an N-type characteristic.

3. The memory device of claim 1, wherein the first dopant having an N-type characteristic and the second dopant having a P-type characteristic.

4. The memory device of claim 1, wherein the first insulator region having a thickness that allows tunneling of charge between the floating gate and the first channel region.

5. The memory device of claim 4, wherein the thickness is between 70 angstroms and 110 angstroms.

6. The memory device of claim 1, wherein the vertical insulator is made from a silicon dioxide having a thickness that provides capacitance between the floating gate and the control gate and prevents leakage between the floating gate and the control gate.

7. The memory device of claim 1, wherein the first vertical insulator is made from an oxide nitrite oxide having a thickness that provides capacitance between the floating gate and the control gate and prevents leakage between the floating gate and the control gate.

8. The memory device of claim 1, wherein the floating gate and the control gate are wrapped by a spacer.

9. The memory device of claim 1, wherein the second diffusion is in contact with a vertical connector, the vertical connector being separated from the control gate by a second vertical insulator.

10. The memory device of claim 9, wherein charge is transported from the first channel region to the floating gate when a first combination of voltages is applied to the first diffusion region, the second diffusion region, the control gate, and the second semiconductor layer.

11. The memory device of claim 10, wherein the first combination of voltages comprises:

applying a positive high voltage to the second semiconductor layer;

applying a positive high voltage to the first diffusion region;

applying zero voltage to the second diffusion region; and

applying a positive high ramp down voltage followed by a ramp up voltage to the control gate.

12. The memory device of claim 10, wherein the first combination of voltages comprises:

applying a positive voltage between 1V and Vpp to the control gate;

applying a zero voltage to the first diffusion region;

applying a positive high voltage to the second diffusion region; and

applying a positive voltage between 0V to Vcc to the second semiconductor layer.

13. The memory device of claim 9, wherein charge inside the floating gate can be determined when a first combination of voltages is applied to the first diffusion region, the control gate, and the second semiconductor layer.

14. The memory device of claim 13, wherein the first combination of voltages comprises:

applying a Vcc voltage to the second semiconductor layer;

applying a Vcc voltage to the first diffusion region; and

applying a voltage between -2V and Vcc to the control gate.

15. The memory device of claim 1, wherein the first diffusion is in contact with a vertical connector, the vertical connector being separated from the floating gate by a second vertical insulator.

16. The memory device of claim 15, wherein charge is transported from the first channel region to the floating gate when a second combination of voltages is applied to the first diffusion region, the control gate, and the second semiconductor layer.

17. The memory device of claim 16, wherein the second combination of voltages comprises:

applying a positive high voltage to the control gate;

applying a negative voltage to the first diffusion region; and

applying a Vcc voltage to the second semiconductor layer.

18. The memory device of claim 16, wherein the second combination of voltages comprises:

applying a positive high voltage to the control gate;

applying a negative voltage to the first diffusion region; and

applying a negative voltage to the second semiconductor layer.

19. The memory device of claim 1, wherein charge is transported from the floating gate to the first channel area when a third combination of voltages is applied to the second semiconductor layer, the control gate, and the first diffusion region

20. The memory device of claim 19, wherein the third combination of voltages comprises:

applying a negative voltage to the control gate;

applying a high positive voltage to the second semiconductor layer; and

applying a positive high voltage to the first diffusion region.

21. An electrically erasable programmable memory device, comprising:

a first semiconductor layer doped with a first dopant in a first concentration;

a second semiconductor layer, adjacent the first semiconductor layer, doped with a second dopant that has an opposite electrical characteristic than the first dopant, the second semiconductor layer having a top side;

two spaced-apart diffusion regions embedded in the top side of the second semiconductor layer, each diffusion region doped with the first dopant in a second

concentration greater than the first concentration, the two diffusion regions including a first diffusion region and a second diffusion region, a first channel region defined between the first diffusion region and the second diffusion region;

a floating gate, comprising a conductive material, disposed adjacent the first diffusion region and above the first channel region and separated therefrom by a first insulator region, the floating gate capable of storing electrical charge and having at least two lateral sides; and

a control gate, comprising a conductive material, disposed laterally adjacent the floating gate and surrounding at least two sides of the floating gate and separated therefrom by a vertical insulator layer, the control gate being disposed above the first channel region and separated therefrom by a second insulator region.

22. The memory device of claim 21, wherein the first dopant having a P-type characteristic and the second dopant having an N-type characteristic.

23. The memory device of claim 21, wherein the first dopant having an N-type characteristic and the second dopant having a P-type characteristic.

24. The memory device of claim 21, wherein the first insulator region having a thickness that allows tunneling of charge between the floating gate and the first channel region.

25. The memory device of claim 24, wherein the thickness is between 70 angstroms and 110 angstroms.

26. The memory device of claim 21, wherein the vertical insulator is made from a silicon dioxide having a thickness that provides capacitance between the floating gate and the control gate and prevents leakage between the floating gate and the control gate.

27. The memory device of claim 21, wherein the first vertical insulator is made from an oxide nitrite oxide having a thickness that provides capacitance between the floating gate and the control gate and prevents leakage between the floating gate and the control gate.

28. The memory device of claim 21, wherein the control gate are wrapped by a spacer.

29. The memory device of claim 21, wherein the second diffusion is in contact with a vertical connector, the vertical connector being separated from the control gate by a second vertical insulator.

30. The memory device of claim 29, wherein charge is transported from the first channel region to the floating gate when a first combination of voltages is applied to the first diffusion region, the second diffusion region, the control gate, and the second semiconductor layer.

31. The memory device of claim 30, wherein the first combination of voltages comprises:

applying a positive high voltage to the second semiconductor layer;

applying a positive high voltage to the first diffusion region;

applying zero voltage to the second diffusion region; and

applying a positive high ramp down voltage followed by a ramp up voltage to the control gate.

32. The memory device of claim 30, wherein the first combination of voltages comprises:

applying a positive voltage between 1V and Vpp to the control gate;

applying a zero voltage to the first diffusion region;

applying a positive high voltage to the second diffusion region; and

applying a positive voltage between 0V to Vcc to the second semiconductor layer.

33. The memory device of claim 29, wherein charge inside the floating gate can be determined when a first combination of voltages is applied to the first diffusion region, and the control gate.

34. The memory device of claim 33, wherein the first combination of voltages comprises:

applying a Vcc voltage to the second semiconductor layer;

applying a Vcc voltage to the first diffusion region; and

applying a voltage between -2V and Vcc to the control gate.

35. The memory device of claim 21, wherein the first diffusion is in contact with a vertical connector, the vertical connector being separated from the floating gate by a second vertical insulator.

36. The memory device of claim 35, wherein charge is transported from the first channel region to the floating gate when a second combination of voltages is applied to the first diffusion region, the control gate, and the second semiconductor layer.

37. The memory device of claim 36, wherein the second combination of voltages comprises:

applying a positive high voltage to the control gate;

applying a negative voltage to the first diffusion region; and

applying a Vcc voltage to the second semiconductor layer.

38. The memory device of claim 36, wherein the second combination of voltages comprises:

applying a positive high voltage to the control gate;

applying a negative voltage to the first diffusion region; and

applying a negative voltage to the second semiconductor layer.

39. The memory device of claim 21, wherein charge is transported from the floating gate to the first channel area when a third combination of voltages is applied to the second semiconductor layer, the control gate, and the first diffusion region

40. The memory device of claim 39, wherein the third combination of voltages comprises:

applying a negative voltage to the control gate;

applying a high positive voltage to the second semiconductor layer; and

applying a positive high voltage to the first diffusion region.

41. An electrically erasable and programmable non-volatile memory array with a plurality of memory bytes, comprising:

a plurality of memory cells, each memory cell having

a first connector connected to a drain of a control transistor in the memory cell, wherein the control transistor comprising a control gate disposed laterally adjacent a floating gate, the control gate and the floating gate being disposed between two diffusion regions,

a second connector connected to a gate of the control transistor, and

a third connector connected to a source of the control transistor, wherein the plurality of memory cells are distributed in rows and columns;

a plurality of bit lines, wherein each bit line being connected to the first connector of every memory cell in a column;

a plurality of control lines, where each control line being connected to the second connector of every memory cell in a row; and

a common source line connected to the third connector of every memory cell in the memory array.

42. The memory array of claim 41, wherein eight consecutive bit lines are connected to a charging control line.

43. The memory array of claim 41, wherein charge are stored into a memory byte composed of the plurality of memory cells, the memory cells of the memory byte being disposed in a single well, when a first combination of voltages is applied to a first plurality of bit lines connected to the memory byte, a control line connected to the memory byte, the common source, and the well.

44. The memory array of claim 43, wherein the first combination of voltages comprises:

applying zero voltage to the bit lines;

applying a positive high voltage to the common source;

applying a positive high voltage to the well; and

applying a positive high ramp down voltage followed by a ramp up voltage to the control line.

45. The memory array of claim 43, wherein the first combination of voltages comprises:

applying a negative voltage to the bit lines;

applying a Vcc voltage to the well; and

applying a positive high voltage to the control line.

46. The memory array of claim 43, wherein the first combination of voltages comprises:

applying a positive high voltage to the bit lines;

applying zero voltage to the common source;

applying a voltage between 0V and Vpp to the well; and

applying a voltage between 1V and Vcc to the control line.

47. The memory array of claim 43, wherein the first combination of voltages comprises:

applying a negative voltage to the bit lines;

applying a negative voltage to the well; and

applying a positive high voltage to the control line.

48. The memory array of claim 41, wherein the existence of charge inside a memory byte composed of the plurality of memory cells, wherein the memory cells of the memory byte being disposed in a single well, can be determined when a second combination of voltages is applied to a first plurality of bit lines connected to the memory byte, a control line connected to the memory byte, the common source, and the well.

49. The memory array of claim 48, wherein the second combination of voltages comprises:

applying a voltage between 0V and Vcc to the control line;

applying a Vcc voltage to the well; and

applying a Vcc voltage to the common source.